Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DONALD GEORGE MIKAN, JR.

Appeal No. 2001-1189
Application No. 08/824,140

ON BRIEF

Before THOMAS, HAIRSTON, and BARRY, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1, 2, 4 through 10, 12 through 18 and 20 through 27.

The disclosed invention relates to a dynamic logic circuit.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A dynamic logic circuit operable for reset during a precharge clock phase and to evaluate during an evaluate clock phase comprising:

first and second NFETs coupled in series between a first node and a first reference voltage, wherein gate electrodes of said first and second NFETs are operable for receiving a data input;

a first PFET coupled between a second reference voltage and a second node coupling said first and second NFETs, wherein a gate electrode of said first PFET is operable for receiving said data input, so that said first and second NFETs and first PFET reduce susceptibility to erroneous discharge of said first node during said evaluate phase; and

a third NFET coupled between said second NFET and said first reference voltage, wherein said third NFET is operable for receiving a clock signal.

The references relied on by the examiner are:

Lyon	5,440,243	Aug. 8, 1995
D'Souza et al. (D'Souza)	5,546,022	Aug. 13, 1996

Claims 1, 2, 4 through 10, 12 through 18[1] and 20 through 27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lyon in view of D'Souza.

[1] If claims 17 and 18 are supposed to be read on the Figure 6 embodiment of a multiplexer circuit, then we question the written description and the definiteness of the claim 17 and claim 18 limitation of "third and fourth NFETs coupled in series between said first node and said first reference voltage, wherein gate electrodes of said third and fourth NFETs are operable for receiving a second data input." This claim limitation cannot be read on such a multiplexer circuit.

Reference is made to the briefs (paper numbers 18 and 22) and the answer (paper number 21) for the respective positions of the appellant and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the obviousness rejection of claims 1, 2, 4 through 10, 12 through 18 and 20 through 27.

According to the examiner (answer, pages 3 and 4), Lyon discloses (prior art Figure 1a) "a dynamic logic circuit operable for reset during a precharge clock phase (when CLK is low) and to evaluate during an evaluate clock phase (when CLK is high), comprising: a first NFET (13a) coupled in series between a first node and a first reference voltage (ground) wherein gate electrode of the first NFET is operable for receiving a data input (InA); a third NFET (12) coupled between the NFET and a reference voltage (ground) and receiving a clock signal (CLK)." The examiner acknowledges (answer, page 4) that "Lyon's prior art figure 1 does not teach the claimed second NFET and first PFET . . . . " The examiner additionally states (answer, page 4) that:

> In figure 4, D'Souza shows a standard MOS logic structure wherein the typical parallel pull-down N-channel MOSFETs are replaced by 2 NFETs and 1 PFET

> connected identically as the claimed first and second NFETs and first PFET. This three transistor structure is an input switch structure receiving a signal input. It is taught as improving the output signal levels of the logic circuitry it is applied to and as reducing leakage current (see, for example, column 1, line 65 - column 2, line 9).

Based upon the teachings of the applied references, the examiner concludes (answer, page 4) that "it would have been obvious to one of ordinary skill in the art at the time of appellant's invention to have replaced the input transistor (13a) of the dynamic MOS logic circuit of Lyon's prior art figure 1 with the three transistor structure (i.e.[,] 422a, 424a, 426a of figure 4) as taught by D'Souza in order to provide a dynamic MOS logic circuit with improved output signal levels and lower leakage current."

Appellant argues (reply brief, pages 2 through 6, 9 and 10) that Lyon is directed to dynamic logic circuits, whereas D'Souza is directed to static logic circuits, and that the skilled artisan would not resort to the static logic teachings of D'Souza to modify the dynamic logic teachings of Lyon. To be more specific, appellant argues (reply brief, page 5) that "the Examiner has not provided objective evidence that the teaching in *D'Souza* does function in a dynamic logic circuit, such as that

taught in *Lyon*, 'to reduce leakage current and improve output signal levels.'" A concluding argument made by appellant (brief, page 19) is that:

> Accordingly, . . . the Examiner cannot establish obviousness by locating references which describe various aspects of the patent Applicant's invention without also providing evidence of the motivating force which would impel one skilled in the art to do what the patent applicant has done. For the aforesaid reasons, [t]he Applicant respectfully asserts that the rejection of Claims 1, 2, 4-10, 12-18 and 20-27 is based on classic hindsight reconstruction, and as evidenced hereinabove, an artisan of ordinary skill, not having the benefit of the Application as a "blueprint", would not be led to combine *Lyon* and *D'Souza* to make the inventions of Claims 1, 2, 4-10, 12-18 and 20-27.

The record before us is silent as to all of the reasons expressed by the examiner for combining the teachings of Lyon and D'Souza. The factual question of motivation should be resolved based on evidence of record, and not on the subjective belief and unknown authority expressed by the examiner. In re Lee, 277 F.3d 1338, 1343-44, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002). Thus, the obviousness rejection of claims 1, 2, 4 through 10, 12 through 18 and 20 through 27 is reversed because we agree with appellant's arguments supra and the argument (brief, page 11; reply brief, page 2) that the examiner has not made a prima facie showing of obviousness.

DECISION

The decision of the examiner rejecting claims 1, 2, 4 through 10, 12 through 18 and 20 through 27 under 35 U.S.C. § 103(a) is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)	
KENNETH W. HAIRSTON Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
LANCE LEONARD BARRY Administrative Patent Judge	)	

KWH:hh

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